



User's Manual

The iPORT™

PT1000-LV IP Engine

February 6, 2006

Rev 060206



These products are not intended for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Pleora Technologies Inc. (Pleora) customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Pleora for any damages resulting from such improper use or sale.

© 2004-2006 Pleora Technologies Inc. All information provided in this manual is believed to be accurate and reliable. No responsibility is assumed by Pleora for its use. Pleora reserves the right to make changes to this information without notice. Redistribution of this manual in whole or in part, by any means, is prohibited without obtaining prior permission from Pleora.

Table of Contents

1.0	Introduction	5
1.1	The Scope of this User's Manual.....	5
1.2	Related Documents	5
2.0	Overview of the iPORT PT1000-LV.....	6
2.1	Highlights.....	6
2.2	Models.....	6
2.3	Characteristics and Features	7
3.0	Camera Configuration and Control	8
4.0	Connectors.....	9
4.1	LVDS Camera Connector	9
4.2	Power and IO Connectors	12
4.2.1	Power Connector for OEM Board Set	12
4.2.2	IO Connector for OEM Board Set	13
4.2.3	Power Connector for Boxed Unit	13
4.2.4	IO Connector for Boxed Unit	14
5.0	Signal Handling	15
5.1	GPIO Control Block	15
5.2	GPIO Programming Signals	17
5.3	Camera Interface.....	18
5.3.1	Camera Inputs	18
5.3.2	Camera Controls	18
5.3.3	Pixel Bus Definition.....	18
6.0	Mechanical Dimensions.....	20
6.1	Mechanical Drawings of OEM Board Set	20
6.2	Mechanical Drawings of Boxed Unit	22
7.0	Additional Support.....	24
7.1	Revision History	24
8.0	Appendix: Legacy Models	25
8.1	Characteristics and Features	26
8.2	GPIO Control Block	27

List of Figures

Figure 1: LVDS Camera Connector	9
Figure 2: Power and IO Connector Locations for OEM Board Set.....	12
Figure 3: Power Connector for Boxed Unit.....	13
Figure 4: IO Connector for Boxed Unit.....	14
Figure 5: iPORT PT1000-LV-V2 GPIO Control Block.....	16
Figure 6: Isometric View of the OEM Board Set	20
Figure 7: Side View of the OEM Board Set	21
Figure 8: Top View of the OEM Board Set.....	21
Figure 9: Front View of the Boxed Unit.....	22
Figure 10: Rear View of the Boxed Unit.....	22
Figure 11: Side View of the Boxed Unit	23
Figure 12: Top View of the Boxed Unit	23
Figure 13: iPORT PT1000-LV GPIO Control Block	27

List of Tables

Table 1: iPORT PT1000-LV-V2 Characteristics and Features	7
Table 2: Camera Connector Pin-Out.....	10
Table 3: LVDS Signal Description	11
Table 4: Power Connector Pin-Out for OEM Board Set	12
Table 5: IO Connector Pin-Out for OEM Board Set	13
Table 6: Power Connector Pin-Out for Boxed Unit.....	14
Table 7: IO Connector Pin-Out for Boxed Unit.....	14
Table 8: iPORT PT1000-LV-V2 GPIO Input Signals	17
Table 9: iPORT PT1000-LV-V2 GPIO Output Signals	17
Table 10: Grabber Interface Pixel Bus Definition	19
Table 11: iPORT PT1000-LV Characteristics and Features.....	26

1.0 Introduction

1.1 The Scope of this User's Manual

This User's Manual describes how to access and use features specific to Pleora's iPORT PT1000-LV IP Engine. The engine is available as both a boxed unit and an OEM board set. Therefore, some of the descriptions in the manual, particularly those dealing with physical aspects, have two sections, one for each form factor of the engine.

1.2 Related Documents

The iPORT PT1000-LV IP Engine is a member of Pleora's growing family of iPORT IP Engines. For information about other available engine models, visit www.pleora.com. All the engines share one set of core features, described in a document entitled "User's Manual, Shared Features of iPORT IP Engines."

The iPORT PT1000-LV IP Engine is one element of the iPORT Connectivity Solution. As such, it is shipped with two PC applications: the iPORT IP Device Driver; and the iPORT Software Development Kit (SDK – available in C++ or Visual Basic). These software applications have their own documentation.

The iPORT Connectivity Solution also includes the iPORT High Memory Manager, which is described in the iPORT IP Device Drivers manual. As an option, the solution can also include iPORT Hydra™ PC Communications Software, described in the SDK C++ manual.

In summary, this User's Manual complements, and should be used in conjunction with, up to four other documents:

- User's Manual, Shared Features of iPORT IP Engines;
- User's Manual, iPORT IP Device Drivers;
- Reference Manual, The iPORT C++ Software Development Kit; and
- Reference Manual, The iPORT Visual Basic Software Development Kit.

2.0 Overview of the iPORT PT1000-LV

2.1 Highlights

The iPORT PT1000-LV delivers the core set of features offered in all iPORT IP Engines, plus a connector and extended functions tailored specifically for LVDS cameras. The engine interfaces to a range of LVDS cameras, including both 1-tap and 2-tap models.

The PT1000-LV streams up to 1 Gb/s of imaging data to PCs in real-time over either point-to-point Gigabit Ethernet (GigE) links or standard GigE LANs. A built-in frame grabber removes horizontal and vertical blank times, which helps maximize bandwidth usage in the GigE connection.

The PT1000-LV also handles control signals from the PC and other system elements. These signals are routed through a PLC (programmable logic controller) that allows users to precisely measure and control the operation of conveyors, encoders, cameras, and other components – either independently from or in conjunction with the host PC on the network.

LVDS cameras do not have a standard cable pin-out. As a result, a custom cable may be required to ensure that signals from the camera feed into the correct inputs on the iPORT PT1000-LV IP Engine. Refer to Section 4.1 of this manual, which describes the LVDS camera connector, for further details.

As one element of Pleora's end-to-end iPORT Connectivity Solution, the PT1000-LV is shipped with two powerful PC applications. The iPORT IP Device Driver (users can choose from two versions: the iPORT High-Performance IP Device Driver or the iPORT Universal IP Filter Driver) streams data to PC memory using minimal CPU capacity. The iPORT SDK gives users the building blocks needed to quickly and easily enable third-party or custom video applications. For more information about the iPORT Connectivity Solution, see the "User's Manual, Shared Features of iPORT IP Engines."

2.2 Models

The standard model of the iPORT PT1000-LV IP Engine is known as the iPORT PT1000-LV-V2. It is available in two variants, each of which has its own order code:

- The LV644 variant, which accepts the signaling levels defined in the TIA/EIA-644 interface standard (i.e. traditional LVDS signaling) on its LVDS camera connector; and
- The RS422 variant, which accepts the signaling levels defined in the TIA/EIA-422-B (RS-422) interface standard on its LVDS camera connector.

Aside from camera connector signaling levels, these variants are exactly the same.

Note: Information about the first-generation version of the iPORT PT1000-LV, known simply as the iPORT PT1000-LV, is described in the Appendix. This model is not available to new customers and is no longer being upgraded with new features.

2.3 Characteristics and Features

Table 1 lists key characteristics and features of the iPORT PT1000-LV-V2.

Hardware		Frame Grabber	
Available as OEM	Yes	Ethernet Bandwidth	1 Gb/s
Available as Boxed	Yes	Unicast	Yes
Onboard Memory	16 MB (Std)	Multicast	Yes
	64 MB (Opt)	Static Configuration	Yes (4.01)
	128 MB (Opt)	BOOTP	Yes
Inputs/Outputs		DHCP	Yes (4.06)
TTL Inputs	2	Number of Data Channels	1
TTL Outputs	2	Video Sources per Data Channel	Up to 3
Optically Isolated Inputs	1	Video Input	EIA-644 (Std) RS-422 (Opt)
Optically Isolated Outputs	1	Progressive Scan	Yes
Camera Control Outputs	4 x LVDS	Area Scan	Yes
Programmable Logic Control		Line Scan	Yes
Pulse Generators (timers)	4	Color	RGB Bayer
Rescaler (16-bit)	1	Monochrome	Yes
Delayers	1	PT1000-LV-V2 Data Output Formats	Grayscale Bayer RGB
General Purpose Counters	1	Pixel Depth (bits)	8, 10, 12, 14, 16, 24
Input Debouncing	Yes	Pixel Clock	Min: 1 MHz Max: 80 MHz
Timestamp Generator	Yes	Taps per Data Channel	2 (Note 1)
Timestamp Trigger	Yes	Image Width (pixels) (must be multiple of 4)	Min: 4 Default: 640 Max: 16,380
Software Controlled IO	4	Image Height (pixels)	Min: 1 Default: 480 Max: 16,383
GPIO Interrupts FIFO	Yes	Windowing	Yes
Other		Decimation	Yes
Serial Ports (UART)	1 x RS232 (Cam.) (Note 6) 1 x RS232 (GPIO)	Decimation by Block	Yes
PT1000-LV-V2 Supply Voltage	Min: 4.5 V Typ: 5 V Max: 16 V	Tap Reconstruction	Optional (Note 4)
Power Consumption (measured at 10V)	EIA-644: Typ: 3.1 W, Max: 3.1 W RS-422: Typ: 3.0 W, Max: 3.0 W	Data Port Mapping	Yes
Operating Temperature	Min: 0 °C Max: 70 °C	Pixel Shifting	Yes
Storage Temperature	Min: -40 °C Max: 125 °C	Pixel Inversion	Yes
		Recording	Yes

Notes:

(x.xx) - Available since firmware version x.xx

NA - Not applicable

* All features supported by iPORT S/W 2.2.0

1 - RGB supported as single-tap, 24 bits

4 - NRE or other charges may apply. Contact Pleora.

6 - Single UART available, multiplexed via SDK

Table 1: iPORT PT1000-LV-V2 Characteristics and Features

3.0 Camera Configuration and Control

Both the PT1000-LV-V2 and the camera to which it is attached are configured by the Camera Configuration Dialog of the iPORT SDK. The PT1000-LV-V2 panels in the dialog are auto-generated by the SDK based on the engine's firmware version and model. This is explained in more detail in the Camera Configuration Dialog section of the "User's Manual, Shared Features of iPORT IP Engines."

The iPORT application is equipped with camera modules for a range of different LVDS models. Check the list in the Select Camera Dialog of the Camera Library Controls. If a camera module is available for your LVDS model, then the Camera Configuration Dialog will auto-generate a panel to control your camera. Internally, the camera module converts the controls of that panel to the actual serial port command of the camera.

If no camera-specific module exists for your LVDS model, then you must select the standard LVDS camera module instead. In this case, you have to find the camera's serial port command information in the camera documentation and type it in the Port Communication Panel.

For more information, read the "User's Manual, Shared Features of iPORT IP Engines," and the `CyDeviceExtensionConstants.h` file in the "Reference Guide, iPORT C++ Software Development Kit."

4.0 Connectors

This section describes the LVDS camera connector and the power and IO connectors on the iPORT PT1000-LV-V2. The Ethernet connector is a standard RJ-45 plug.

4.1 LVDS Camera Connector

The OEM and boxed versions of the iPORT PT1000-LV-V2 IP engine both use the same LVDS connector, the Hirose 68-pin female MDR shown in Figure 1. The part number is DX10GM-68SE. The part number for the mating cable is DX30AM-68P, and for the shell is DX30M-68-CV. Table 2 shows how the 68 pins on the connector map to signals and Table 3 describes the function of each type of signal.

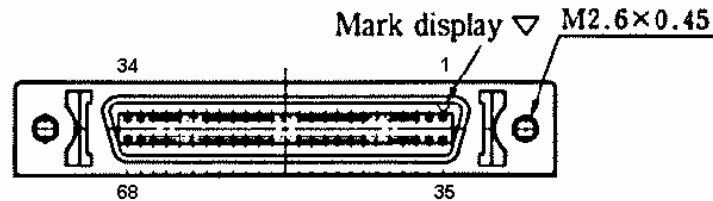


Figure 1: LVDS Camera Connector

Pin	Signal Name	I/O		Pin	Signal Name	I/O
1	GND	-		35	DATA_16+ / GC_0+	IN / OUT
2	DATA_0+	IN		36	DATA_16- / GC_0-	IN / OUT
3	DATA_0-	IN		37	DATA_17+ / GC_1+	IN / OUT
4	DATA_1+	IN		38	DATA_17- / GC_1-	IN / OUT
5	DATA_1-	IN		39	DATA_18+ / GC_2+	IN / OUT
6	DATA_2+	IN		40	DATA_18- / GC_2-	IN / OUT
7	DATA_2-	IN		41	DATA_19+ / GC_3+	IN / OUT
8	DATA_3+	IN		42	DATA_19- / GC_3-	IN / OUT
9	DATA_3-	IN		43	DATA_20+	IN
10	DATA_4+	IN		44	DATA_20-	IN
11	DATA_4-	IN		45	DATA_21+	IN
12	DATA_5+	IN		46	DATA_21-	IN
13	DATA_5-	IN		47	DATA_22+	IN
14	DATA_6+	IN		48	DATA_22-	IN
15	DATA_6-	IN		49	DATA_23+	IN
16	DATA_7+	IN		50	DATA_23-	IN
17	DATA_7-	IN		51	FVAL+	IN
18	DATA_8+	IN		52	FVAL-	IN
19	DATA_8-	IN		53	LVAL+	IN
20	DATA_9+	IN		54	LVAL-	IN
21	DATA_9-	IN		55	DVAL+	IN
22	DATA_10+	IN		56	DVAL-	IN
23	DATA_10-	IN		57	CC1+	OUT
24	DATA_11+	IN		58	CC1-	OUT
25	DATA_11-	IN		59	CC2+	OUT
26	DATA_12+	IN		60	CC2-	OUT
27	DATA_12-	IN		61	CC3+	OUT
28	DATA_13+	IN		62	CC3-	OUT
29	DATA_13-	IN		63	CC4+	OUT
30	DATA_14+	IN		64	CC4-	OUT
31	DATA_14-	IN		65	RS232_RX0	IN
32	DATA_15+	IN		66	RS232_TX0	OUT
33	DATA_15-	IN		67	CLK_IN+	IN
34	GND	-		68	CLK_IN-	IN

Table 2: Camera Connector Pin-Out

Signal Name	Type	Description
GND	PWR	Ground.
DATA[23:0]	IN	LVDS Data In. When interfacing to 2-tap cameras, please refer to Table 10 for the Pixel Bus Definition. A[11:0] is for the first tap, B[11:0] is for the second. DATA[19:16] are input signals when configured as inputs. They are not available when the GC[3:0] (GPIO_CTRL) signals are used as outputs. Refer to the GC[3:0] signal entry in this table for details on how to use them as outputs.
FVAL	IN	LVDS Frame Valid. Polarity (high or low) and mode (level or edge) can be programmed via the SDK.
LVAL	IN	LVDS Line Valid. Polarity (high or low) and mode (level or edge) can be programmed via the SDK.
DVAL	IN	LVDS Data Valid. Polarity (high or low) and mode (level or edge) can be programmed via the SDK.
CLK_IN	IN	LVDS Clock In. Data and control signals are latched on rising edge. Max: 66 MHz
CC[4:1]	OUT	LVDS Camera Control. These outputs come from the Look-Up Table Q[7:4] in the GPIO Control Block. The Look-Up Table is programmable via a dialog in the SDK.
GC[3:0]	OUT	LVDS GPIO Control. These outputs come from the GPIO_CTRL[3:0] register in the GPIO Control Block. They can be individually set and cleared via a dialog in the SDK. GC[3:0] are only available if the DATA[19:16] signals are not used as inputs.
RS232_TX0	OUT	RS-232 Transmit signal from the internal UART0.
RS232_RX0	IN	RS-232 Receive signal to the internal UART0.

Table 3: LVDS Signal Description

4.2 Power and IO Connectors

4.2.1 Power Connector for OEM Board Set

The iPORT PT1000-LV-V2 OEM board set accepts power supply voltages of from 4.5 V to 16 V (regulated). The connector, shown as J2 on the left-hand side of Figure 2, is a Molex 4-pin 6373 Series (22-23-2041). The part mates with the Molex 4-pin shell (22-01-3047) and the Molex crimp pin (08-55-0102). Table 4 lists the four pins in this connector and describes the function of each.

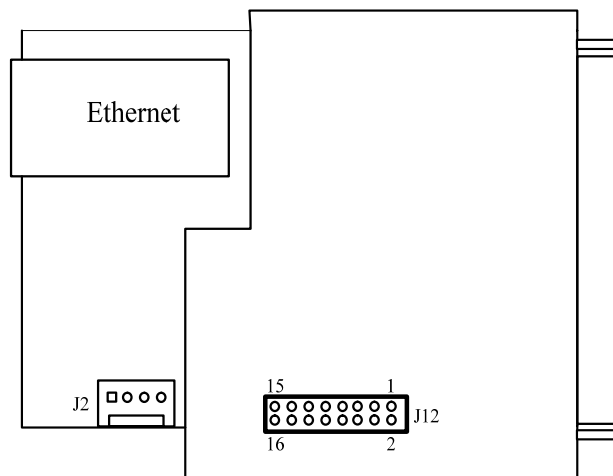


Figure 2: Power and IO Connector Locations for OEM Board Set

Pin	Signal Name	Type	Description
1	GND	PWR	Ground
2	VIN	PWR	Power supply voltage in (4.5 V to 16 V regulated)
3	VIN	PWR	Power supply voltage in (4.5 V to 16 V regulated)
4	GND	PWR	Ground

Table 4: Power Connector Pin-Out for OEM Board Set

4.2.2 IO Connector for OEM Board Set

The IO connector for the iPORT PT1000-LV-V2 OEM board set is a 16-pin, Samtec 2 mm male header (TMM-108-01-G-D-SM). The mating connectors are in the Samtec MMS-108-02-xx-xx series. The mating flat cables are in the Samtec TCSD series (TCSD-08-xxxxxxx). The IO connector is shown as J12 on the right-hand side of Figure 2. Table 5 lists the 16 pins in the connector and describes the function of each.

Pin	Signal Name	Description
1	GND	Ground
2	VCC	3.3 V at 250 mA max*
3	OPT0_OUT-	Optically isolated negative output
4	OPT0_OUT+	Optically isolated positive output
5	TTL_IN[0]	TTL input 0
6	TTL_OUT[0]	TTL output 0
7	TTL_OUT[1]	TTL output 1
8	TTL_IN[1]	TTL input 1
9	N/C	No connect (leave unconnected)
10	N/C	No connect (leave unconnected)
12	OPT0_IN-	Optically isolated negative input
12	OPT0_IN+	Optically isolated positive input
13	RS232_RX1	RS-232 RX 1
14	RS232_TX1	RS-232 TX 1
15	GND	Ground
16	VCC	3.3 V at 250 mA max*

Table 5: IO Connector Pin-Out for OEM Board Set

4.2.3 Power Connector for Boxed Unit

The boxed version of the iPORT PT1000-LV-V2 uses a Hirose 6-pin power connector, as shown in Figure 3. The part number for this connector is HR10A-7R-6P; its mating part number is HR10A-7P-6S. Table 6 lists the six pins in the connector and describes the function of each.

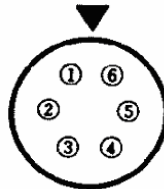


Figure 3: Power Connector for Boxed Unit

* These VCC supplies are not recommended for analog circuitry. Analog circuitry should be driven from a separate 3.3 V supply.

Pin	Description
1	VIN 4.5 V to 16 V regulated
2	VIN 4.5 V to 16 V regulated
3	VIN 4.5 V to 16 V regulated
4	Ground
5	Ground
6	Ground

Table 6: Power Connector Pin-Out for Boxed Unit

4.2.4 IO Connector for Boxed Unit

The boxed version of the iPORT PT1000-LV-V2 uses a Hirose 12-pin connector, as shown in Figure 4. The part number for this connector is HR10A-10R-12S; the mating part number is HR10A-10P-12P. Table 7 lists the 12 pins in the connector and describes the function of each.

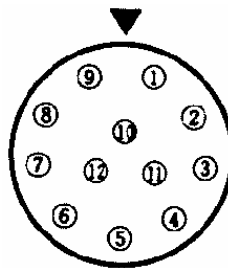


Figure 4: IO Connector for Boxed Unit

Pin	Signal Name	Description
1	OPT0_OUT-	Optically isolated negative output
2	OPT0_OUT+	Optically isolated positive output
3	TTL_IN[0]	TTL input 0
4	TTL_OUT[0]	TTL output 0
5	TTL_OUT[1]	TTL output 1
6	TTL_IN[1]	TTL input 1
7	OPT0_IN-	Optically isolated negative input
8	OPT0_IN+	Optically isolated positive input
9	RS232_RX1	RS-232 RX 1
10	RS232_TX1	RS-232 TX 1
11	GND	Ground
12	VCC	3.3 V at 100 mA max

Table 7: IO Connector Pin-Out for Boxed Unit

5.0 Signal Handling

The iPORT PT1000-LV-V2 handles the signals in much the same way as other iPORT IP engine models. There are a few minor differences, which are described in this section.

5.1 GPIO Control Block

The Programmable Logic Controller (PLC) in the iPORT PT1000-LV-V2 routes signals through a sophisticated GPIO Control Block. Figure 5 shows the GPIO Control Block for the iPORT PT1000-LV-V2. For further details on how the engines handle IO signals, see the “User’s Manual, Shared Features of iPORT IP Engines.”

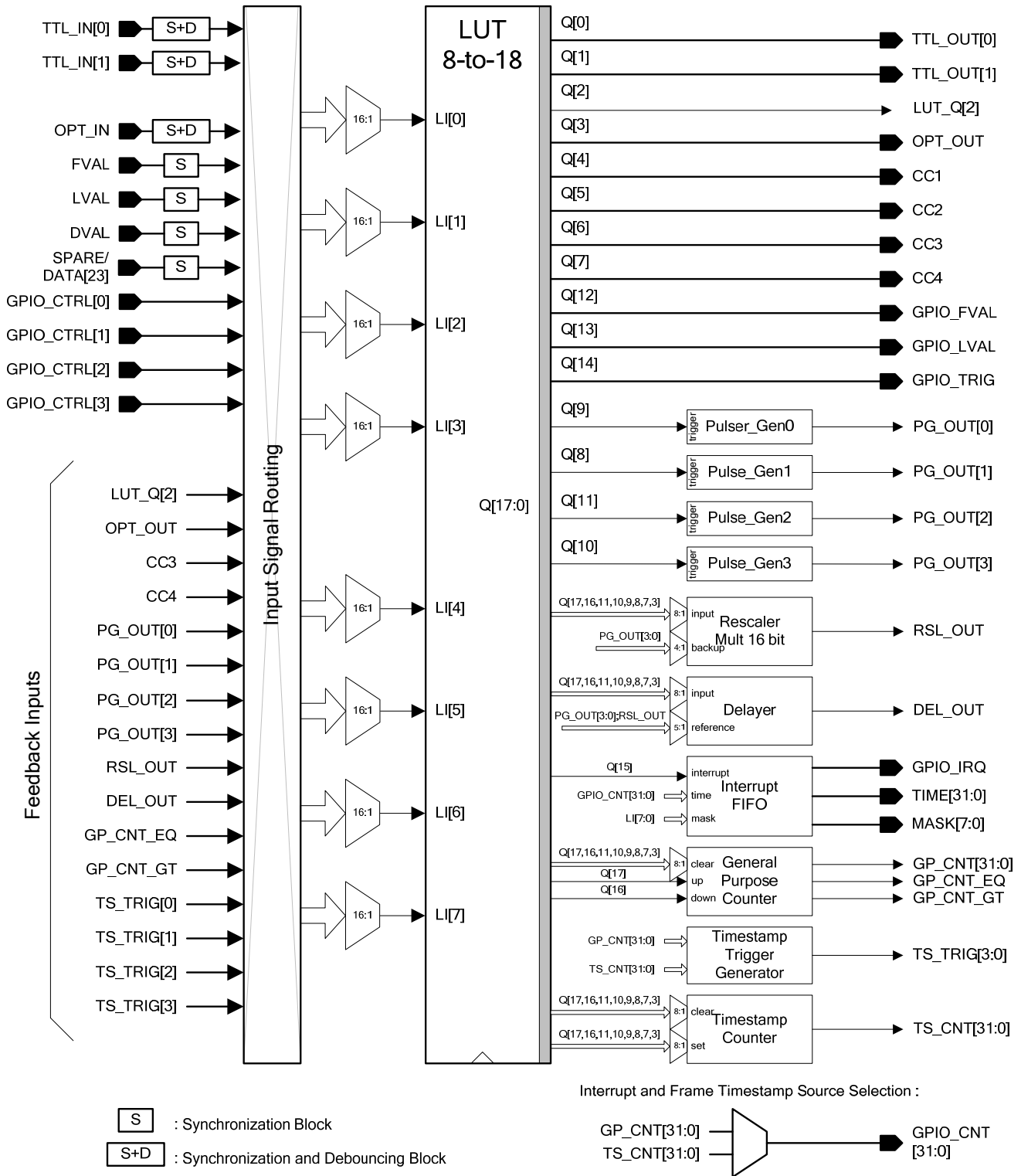


Figure 5: iPORT PT1000-LV-V2 GPIO Control Block

5.2 GPIO Programming Signals

Table 8 lists the input programming signals that are specific to the iPORT PT1000-LV-V2. The labels for these signals in the GPIO Look-Up Table depend on the configuration of the GPIO Look-Up Table dialog in the iPORT SDK. See the “User’s Manual, Shared Features of iPORT IP Engines” for details about other GPIO programming signals used by the engine.

Table 9 lists the output programming signals that are specific to the iPORT PT1000-LV-V2, as well as the GPIO labels for these signals in the GPIO Look-Up Table.

Input Signal	Description
TTL_IN[0]	TTL input 0
TTL_IN[1]	TTL input 1
OPTO_IN	Optically isolated input
FVAL	Frame Valid signal. Refer to camera documentation to find out how specific cameras handle this signal.
LVAL	Line Valid signal. Refer to camera documentation to find out how specific cameras handle this signal.
DVAL	Data Valid signal. Refer to camera documentation to find out how specific cameras handle this signal.
SPARE/DATA[23]	Spare signal / Data In, bit 23. Can be used as either a camera control in signal or a data in bit. Refer to camera documentation to find out how specific cameras handle this signal.

Table 8: iPORT PT1000-LV-V2 GPIO Input Signals

Output Signal	Label	Description
TTL_OUT[0]	Q0	TTL output 0
TTL_OUT[1]	Q1	TTL output 1
LUT_Q[2]	Q2	Feedback signal into GPIO Look-Up Table
OPT_OUT	Q3	Optically isolated output
CC1	Q4	Camera control 1. Refer to camera documentation to find out how specific cameras handle this signal.
CC2	Q5	Camera control 2. Refer to camera documentation to find out how specific cameras handle this signal.
CC3	Q6	Camera control 3. Refer to camera documentation to find out how specific cameras handle this signal.
CC4	Q7	Camera control 4. Refer to camera documentation to find out how specific cameras handle this signal.

Table 9: iPORT PT1000-LV-V2 GPIO Output Signals

5.3 Camera Interface

5.3.1 Camera Inputs

Most LVDS cameras have three standard signals: frame valid (FVAL), line valid (LVAL), and data valid (DVAL). FVAL and LVAL can be activated by positive or negative signal edges, or by high or low levels. DVAL can be activated by high or low levels. See the “User’s Manual, Shared Features of iPORT IP Engines” for more details. Refer to camera documentation for information on the polarity and type of the signals required to support specific camera models.

5.3.2 Camera Controls

The iPORT PT1000-LV-V2 can send commands to cameras through the Camera Control signals. For information on the availability and function of camera controls, refer to camera documentation.

The labels of the control outputs to the camera in the GPIO Control Block programming language are:

- Q4, for Camera Control 1 (CC1)
- Q5, for Camera Control 2 (CC2)
- Q6, for Camera Control 3 (CC3)
- Q7, for Camera Control 4 (CC4)

5.3.3 Pixel Bus Definition

Table 10 shows the pixel bus definition for the grabber interface, including all the configurations supported. Note that when interfacing to 2-tap cameras, A[11:0] is for the first tap and B[11:0] is for the second.

The grabber input should be configured to match the camera head pixel bus, using the `CY_GRABBER_PARAM_PIXEL_DEPTH` and `CY_GRABBER_PARAM_TAP_QUANTITY` parameters of the `CyGrabber` class in the iPORT SDK. For the RGB configuration, the grabber should be set to 1 tap and 24 bits.

The grabber output can reformat the data using the `CY_GRABBER_PARAM_NORMALIZED` and `CY_GRABBER_PARAM_PACKED` parameters of the `CyGrabber` class. The structure of the resulting buffer is described in the Derived Pixel Type Classes of the Imaging Library section of the “Reference Manual, iPORT C++ Software Development Kit.”

	Signal	Pixel Bus	8-bit	10-bit	12-bit	14-bit	16-bit	RGB
Port A0	DATA_0+/-	DATA[0]	A0	A0	A0	A0	A0	R0
Port A1	DATA_1+/-	DATA[1]	A1	A1	A1	A1	A1	R1
Port A2	DATA_2+/-	DATA[2]	A2	A2	A2	A2	A2	R2
Port A3	DATA_3+/-	DATA[3]	A3	A3	A3	A3	A3	R3
Port A4	DATA_4+/-	DATA[4]	A4	A4	A4	A4	A4	R4
Port A5	DATA_5+/-	DATA[5]	A5	A5	A5	A5	A5	R5
Port A6	DATA_6+/-	DATA[6]	A6	A6	A6	A6	A6	R6
Port A7	DATA_7+/-	DATA[7]	A7	A7	A7	A7	A7	R6
Port B0	DATA_8+/-	DATA[8]	B0	A8	A8	A8	A8	G0
Port B1	DATA_9+/-	DATA[9]	B1	A9	A9	A9	A9	G1
Port B2	DATA_10+/-	DATA[10]	B2	N/C	A10	A10	A10	G2
Port B3	DATA_11+/-	DATA[11]	B3	N/C	A11	A11	A11	G3
Port B4	DATA_12+/-	DATA[12]	B4	B8	B8	A12	A12	G4
Port B5	DATA_13+/-	DATA[13]	B5	B9	B9	A13	A13	G5
Port B6	DATA_14+/-	DATA[14]	B6	N/C	B10	N/C	A14	G6
Port B7	DATA_15+/-	DATA[15]	B7	N/C	B11	N/C	A15	G7
Port C0	DATA_16+/-	DATA[16]	N/C	B0	B0	N/C	N/C	B0
Port C1	DATA_17+/-	DATA[17]	N/C	B1	B1	N/C	N/C	B1
Port C2	DATA_18+/-	DATA[18]	N/C	B2	B2	N/C	N/C	B2
Port C3	DATA_19+/-	DATA[19]	N/C	B3	B3	N/C	N/C	B3
Port C4	DATA_20+/-	DATA[20]	N/C	B4	B4	N/C	N/C	B4
Port C5	DATA_21+/-	DATA[21]	N/C	B5	B5	N/C	N/C	B5
Port C6	DATA_22+/-	DATA[22]	N/C	B6	B6	N/C	N/C	B6
Port C7	DATA_23+/-	DATA[23]	N/C	B7	B7	N/C	N/C	B7

Table 10: Grabber Interface Pixel Bus Definition

6.0 Mechanical Dimensions

This section provides mechanical drawings and measurements of the boxed and OEM versions of the iPORT PT1000-LV-V2 IP Engine. The measurements are in inches unless otherwise noted. The measurements have the following tolerances, depending on the number of significant digits provided:

.X	± 0.1
.XX	± 0.01
.XXX	± 0.005

6.1 Mechanical Drawings of OEM Board Set

Figure 6 to Figure 8 are mechanical drawings of the iPORT PT1000-LV-V2 OEM board set. The main board and daughter board are both 0.063 inches thick. The maximum secondary component height on both boards is 0.08 inches, unless otherwise specified in the drawings.

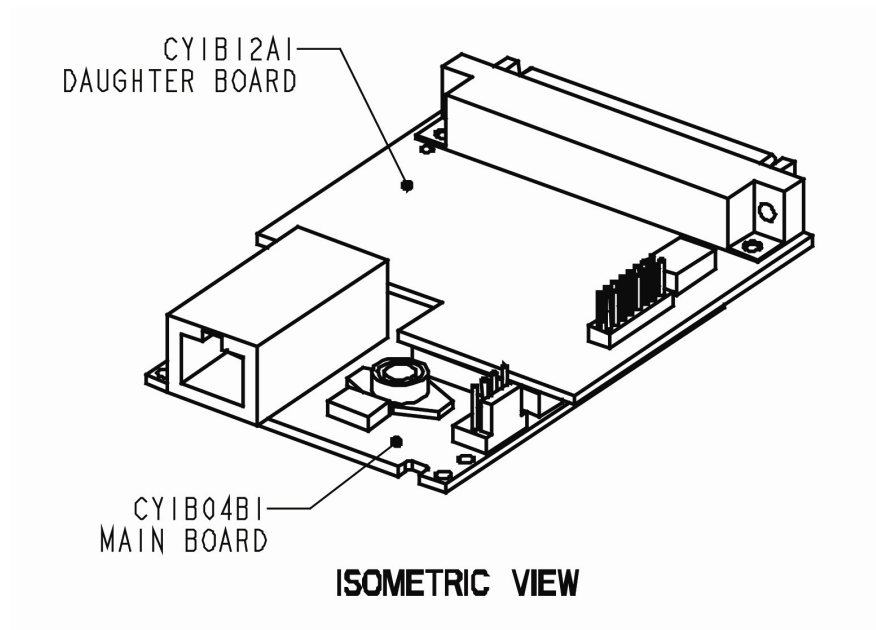


Figure 6: Isometric View of the OEM Board Set

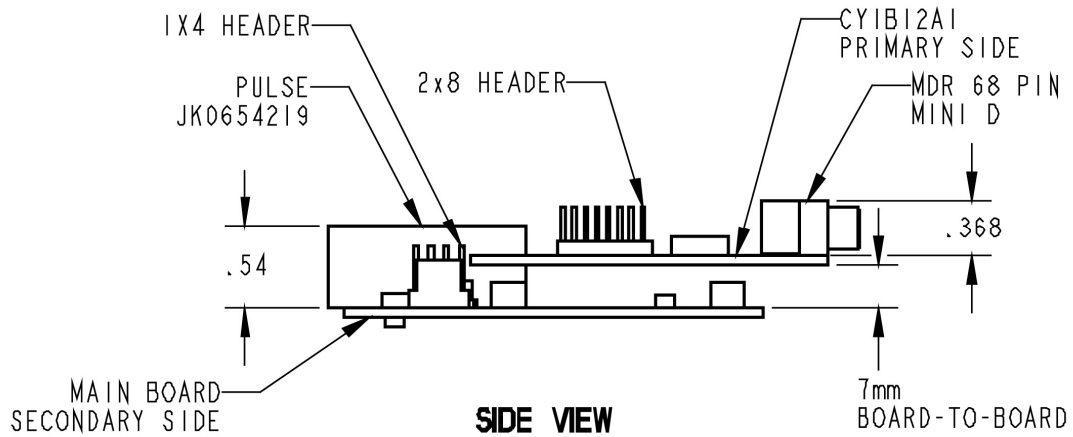


Figure 7: Side View of the OEM Board Set

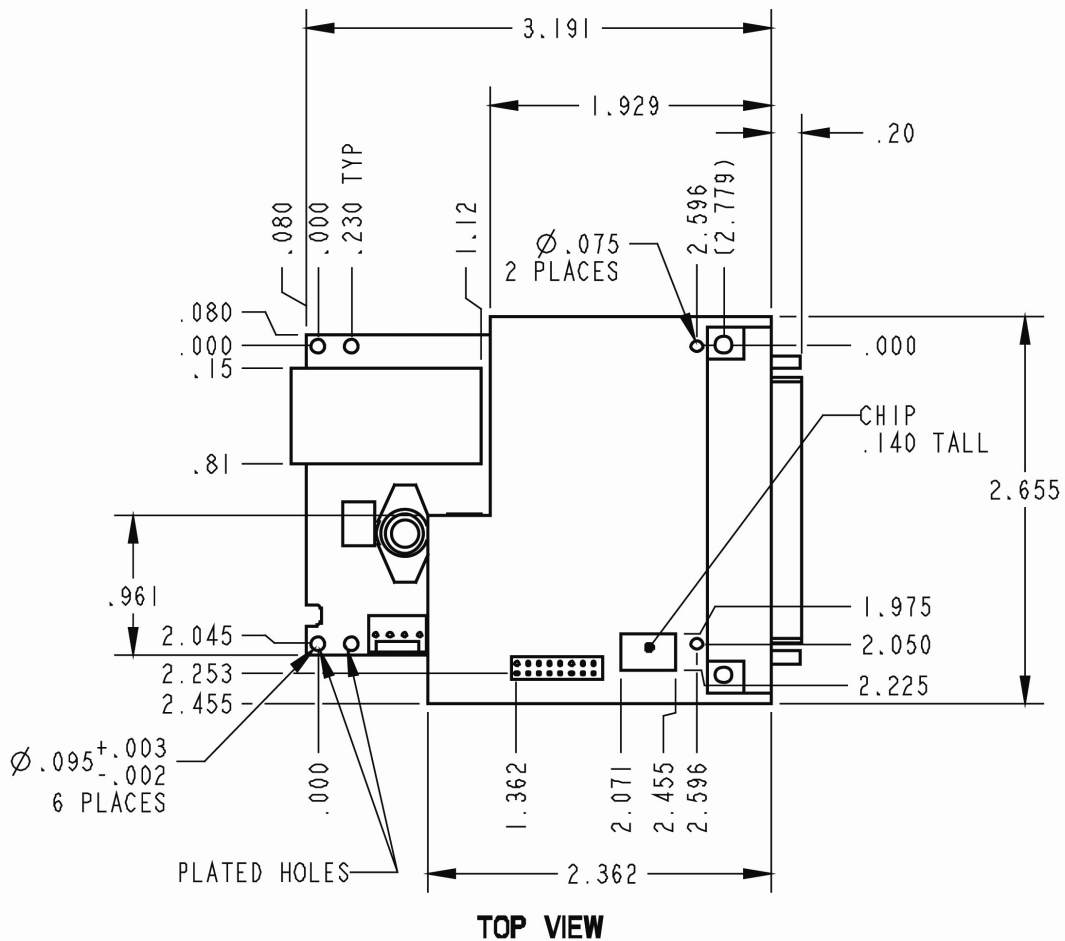


Figure 8: Top View of the OEM Board Set

6.2 Mechanical Drawings of Boxed Unit

The drawings in Figure 9 to Figure 12 show views of the boxed version of the IP engine. The enclosure is made from anodized aluminum and provides four mounting holes. The mounting hole diameter and slot width are both 0.17 +/- 0.01 inches.

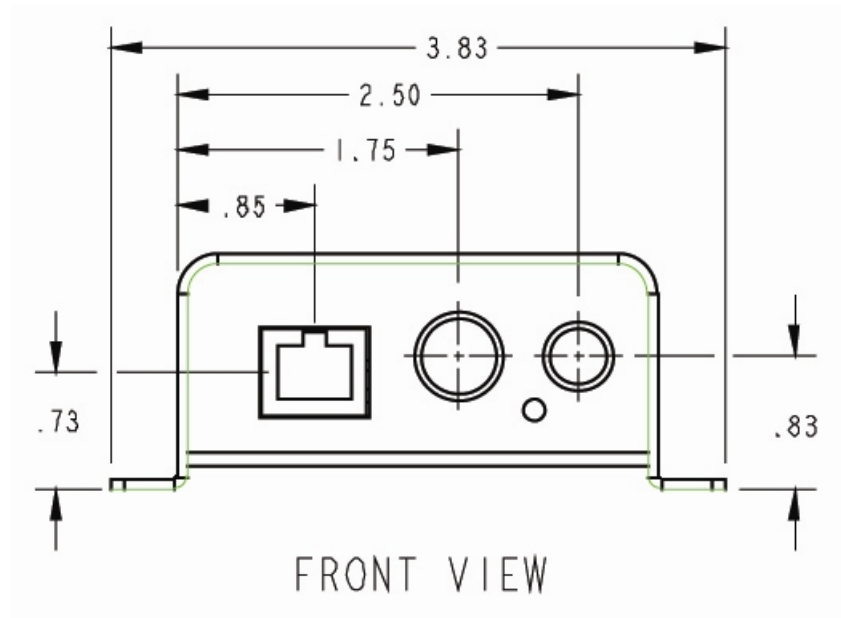


Figure 9: Front View of the Boxed Unit

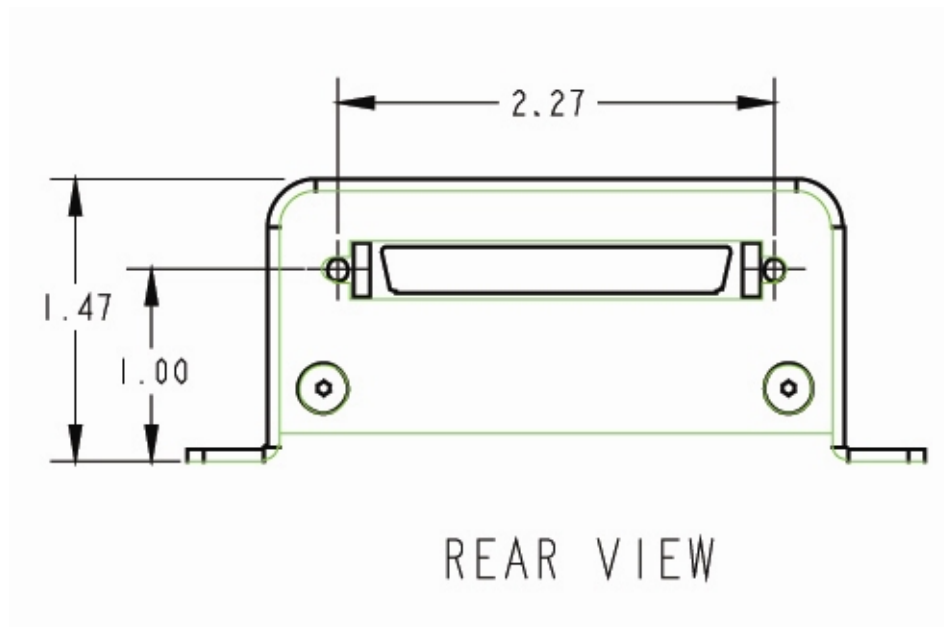
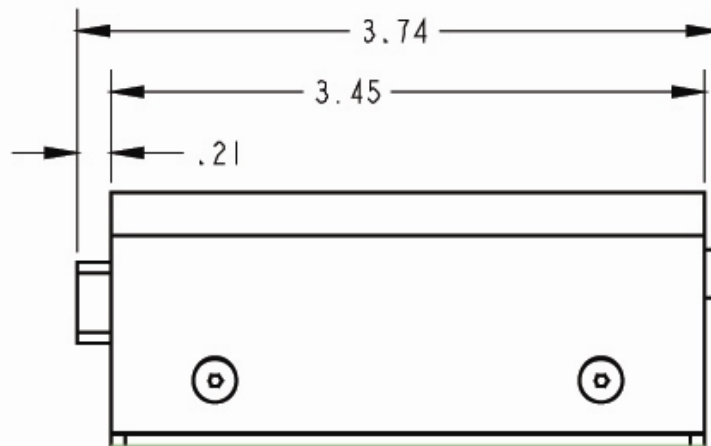
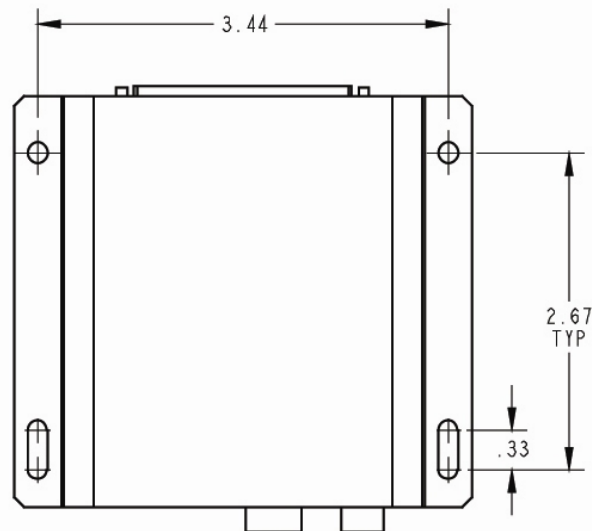


Figure 10: Rear View of the Boxed Unit



SIDE VIEW

Figure 11: Side View of the Boxed Unit



TOP VIEW

Figure 12: Top View of the Boxed Unit

7.0 Additional Support

Additional support can be obtained by contacting Applications Support at Pleora Technologies Inc. at +(613) 270-0625 or by sending an email to support@pleora.com.

7.1 Revision History

Revision	Date	Description
2.1.1	January 2004	- Creation
2.1.3	November 2004	- Updated GPIO diagram - Modified text to reflect iPORT Software 2.1.3
060206	February 2006	- Modified text to reflect iPORT Software V2.2.0 - Added Characteristics and Features table - Added pixel bus definition - Reordered sections - Updated formatting to comply with new Pleora template - Added Revision History table - Created Appendix for legacy models

8.0 Appendix: Legacy Models

This appendix is a brief overview of the features and GPIO block in the first-generation version of the iPORT PT1000-LV IP Engine, known simply as the iPORT PT1000-LV. This model is not available to new customers and is no longer being upgraded with new features. Table 11 lists its key characteristics and features and Figure 13 shows its GPIO Control Block.

8.1 Characteristics and Features

Hardware	
Available as OEM	Yes
Available as Boxed	Yes
Onboard Memory	16 MB (Std) 64 MB (Opt) 128 MB (Opt)
Inputs/Outputs	
TTL Inputs	2
TTL Outputs	2
Optically Isolated Inputs	1
Optically Isolated Outputs	1
Camera Control Outputs	4 x LVDS
Programmable Logic Control	
Pulse Generators (timers)	2
Rescaler (12-bit)	1
Delayers	1
General Purpose Counters	1
Input Debouncing	Yes
Timestamp Generator	Yes
Timestamp Trigger	Yes (3.50)
Software Controlled IO	4
GPIO Interrupts FIFO	Yes (3.50)
Other	
Serial Ports (UART)	1 x RS232 (Cam.) (Note 6) 1 x RS232 (GPIO)
PT1000-LV Supply Voltage	Min: 4.5 V Typ: 5 V Max: 16 V
Power Consumption (measured at 10V)	EIA-644: Typ: 3.1 W, Max: 3.1 W RS-422: Typ: 3.0 W, Max: 3.0 W
Operating Temperature	Min: 0 °C Max: 70 °C
Storage Temperature	Min: -40 °C Max: 125 °C
Notes: (x.xx) - Available since firmware version x.xx NA - Not applicable * All features supported by iPORT S/W 2.2.0 1 - RGB supported as single-tap, 24 bits 6 - Single UART available, multiplexed via SDK	

Frame Grabber	
Ethernet Bandwidth	1 Gb/s
Unicast	Yes
Multicast	Yes
BOOTP	Yes
Number of Data Channels	1
Video Sources per Data Channel	Up to 3
Video Input	EIA-644 (Std) RS-422 (Opt)
Progressive Scan	Yes
Area Scan	Yes
Line Scan	Yes
Color	RGB Bayer
Monochrome	Yes
PT1000-LV Data Output Formats	Grayscale Bayer RGB
Pixel Depth (bits)	8, 10, 12, 14, 16, 24
Pixel Clock	Min: 1 MHz Max: 80 MHz
Taps per Data Channel	2 (Note 1)
Image Width (pixels) (must be multiple of 4)	Min: 4 Default: 640 Max: 16,380
Image Height (pixels)	Min: 1 Default: 480 Max: 16,383
Windowing	Yes
Decimation	Bayer: Yes (3.24) Others: Yes
Decimation by Block	Yes (3.24)
Data Port Mapping	Yes (3.16)
Pixel Shifting	Yes (3.16)
Pixel Inversion	Yes (3.16)
Recording	Yes (3.14)

Table 11: iPORT PT1000-LV Characteristics and Features

8.2 GPIO Control Block

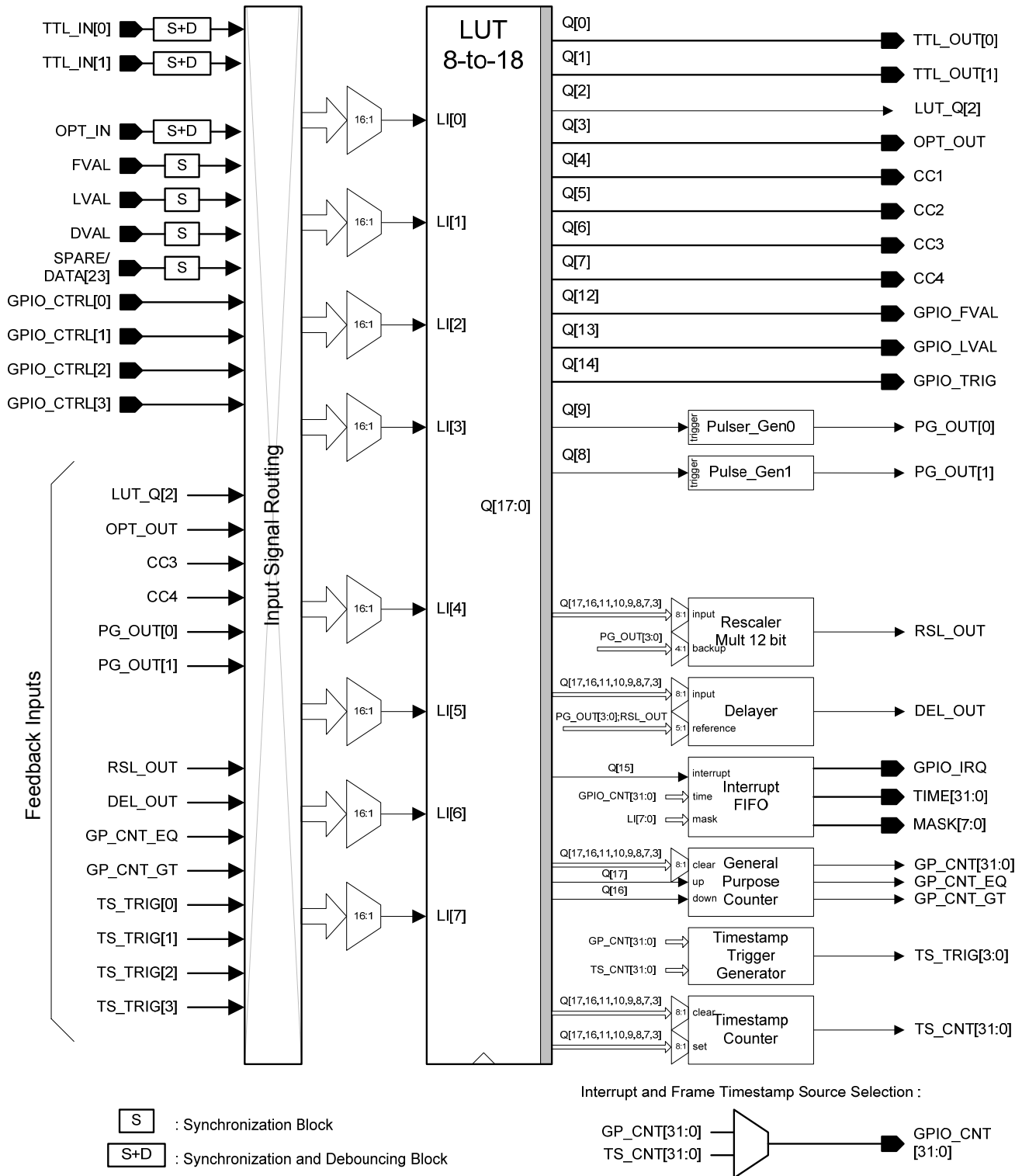


Figure 13: iPORT PT1000-LV GPIO Control Block

